

WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor device having a MIS transistor comprising the steps of:

preparing an epitaxial semiconductor substrate with a multi-layer structure having an epitaxial region formed by epitaxial growing silicon on a silicon substrate;

forming a gate electrode above said epitaxial region with a gate insulating film sandwiched therebetween; and

forming a diffusion layer of said MIS transistor in said epitaxial region, by using a dopant ion having a relatively large mass number,

wherein said diffusion layer is formed shallower than said epitaxial region.

2. The method for fabricating a semiconductor device of Claim 1, wherein said epitaxial region has a $\langle 110 \rangle$ -oriented zone axis.

3. The method for fabricating a semiconductor device of Claim 1, wherein said dopant ion, is an indium ion.

4. The method for fabricating a semiconductor device of Claim 1, wherein said diffusion layer corresponds to a pocket diffusion layer of a MIS transistor, and

the method for fabricating said MIS transistor includes the steps of:

forming said pocket diffusion layer by implanting a first dopant of a first conductivity type corresponding to said dopant ion into said epitaxial region with said gate electrode used as a mask; and

forming an extension diffusion layer by implanting a second dopant of a second conductivity type into said epitaxial region to have shallower junction than said pocket diffusion layer with said gate electrode used as a mask.

5. The method for fabricating a semiconductor device of Claim 4, further comprising a step of forming a channel diffusion layer by implanting a third dopant of the first conductivity type into said epitaxial region before forming said gate electrode.

6. The method for fabricating a semiconductor device of Claim 4, wherein said second dopant is an antimony ion.
7. The method for fabricating a semiconductor device of Claim 3, wherein a dose of said indium ion is $5 \times 10^{13}/\text{cm}^2$ or more.
8. The method for fabricating a semiconductor device of Claim 2, wherein said dopant ion is an indium ion.
9. The method for fabricating a semiconductor device of Claim 3, wherein said diffusion layer corresponds to a pocket diffusion layer of said MIS transistor, and
the method for fabricating said MIS transistor includes the steps of:
forming said pocket diffusion layer by implanting a first dopant of a first conductivity type corresponding to said dopant ion into said epitaxial region with said gate electrode used as a mask; and
forming an extension diffusion layer by implanting a second dopant of a second conductivity type into said epitaxial region to have shallower junction than said pocket diffusion layer with said gate electrode used as a mask.
10. The method for fabricating a semiconductor device of Claim 9, wherein said second dopant is an antimony ion.
11. The method for fabricating a semiconductor device of Claim 1, wherein said dopant is an antimony ion.
12. The method for fabricating a semiconductor device of Claim 1, wherein said diffusion layer is a channel diffusion layer formed below said gate electrode in said epitaxial region.
13. The method for fabricating a semiconductor device of Claim 3, wherein said diffusion layer is a channel diffusion layer formed below said gate electrode in said epitaxial region.

14. The method for fabricating a semiconductor device of Claim 1,
wherein said diffusion layer is a pocket diffusion layer formed on both sides of
said gate electrode in said epitaxial region.

15. The method for fabricating a semiconductor device of Claim 3,
wherein said diffusion layer is a pocket diffusion layer formed on both sides of
said gate electrode in said epitaxial region.

16. A method for fabricating a semiconductor device having a MIS transistor
comprising the steps of:

preparing a semiconductor substrate composed of silicon and having a main
surface of < 100>-orientation;

forming a gate electrode above said semiconductor substrate with a gate
insulating film sandwiched therebetween; and

forming a diffusion layer of said MIS transistor by using a dopant ion having a
relatively large mass number in said semiconductor substrate.

17. The method for fabricating a semiconductor device of Claim 16,
wherein said dopant ion is an indium ion.

18. The method for fabricating a semiconductor device of Claim 16,
wherein said diffusion layer corresponds to a pocket diffusion layer of a MIS
transistor, and

the method for fabricating said MIS transistor includes the steps of:

forming said pocket diffusion layer by implanting a first dopant of a first
conductivity type corresponding to said dopant ion into said semiconductor substrate with
said gate electrode used as a mask; and

forming an extension diffusion layer by implanting a second dopant of a
second conductivity type into said semiconductor substrate to have shallower junction than
said pocket diffusion layer with said gate electrode used as a mask.

19. The method for fabricating a semiconductor device of Claim 18, further
comprising a step of forming a channel diffusion layer by implanting a third dopant of the
first conductivity type into said semiconductor substrate before forming said gate electrode.

20. The method for fabricating a semiconductor device of Claim 18, wherein said second dopant is an antimony ion.
21. The method for fabricating a semiconductor device of Claim 17, wherein a dose of said indium ion is $5 \times 10^{13}/\text{cm}^2$ or more.
22. The method for fabricating a semiconductor device of Claim 17, wherein said diffusion layer corresponds to a pocket diffusion layer of said MIS transistor, and
the method for fabricating said MIS transistor includes the steps of:
forming said pocket diffusion layer by implanting a first dopant of a first conductivity type corresponding to said dopant ion into said semiconductor substrate with said gate electrode used as a mask; and
forming an extension diffusion layer by implanting a second dopant of a second conductivity type into said semiconductor substrate to have shallower junction than said pocket diffusion layer with said gate electrode used as a mask.
23. The method for fabricating a semiconductor device of Claim 22, wherein said second dopant is an antimony ion.
24. The method for fabricating a semiconductor device of Claim 16, wherein said dopant is an antimony ion.
25. The method for fabricating a semiconductor device of Claim 17, wherein said diffusion layer is a channel diffusion layer formed below said gate electrode in said semiconductor substrate.
26. The method for fabricating a semiconductor device of Claim 17, wherein said diffusion layer is a pocket diffusion layer formed on both sides of said gate electrode in said semiconductor substrate.
27. The method for fabricating a semiconductor device of Claim 16, wherein said silicon substrate has a CZ crystal substrate formed by using a CZ method.

28. A method for fabricating a semiconductor device having a MIS transistor comprising:

a step of forming a diffusion layer of said MIS transistor by implanting a dopant ion having a relatively large mass number into said semiconductor substrate at a current density of approximately $100 \mu\text{A}/\text{cm}^2$ or less.

29. The method for fabricating a semiconductor device of Claim 28, wherein said dopant ion is an indium ion.

30. A method for fabricating a semiconductor device having a MIS transistor comprising:

a step of forming a diffusion layer of said MIS transistor by implanting a dopant ion having a relatively large mass number into said semiconductor substrate at an angle of approximately 30 degree or more against a vertical direction to a substrate surface of said semiconductor substrate.

31. The method for fabricating a semiconductor device of Claim 30, wherein said dopant ion is an indium ion.